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REMARKS

Claims 1-4 are pending in the application. Claim 1 has been amended by the present amendment to specify the order of steps. The amendment is fully supported by the application as originally filed.

Applicants' claimed invention is directed to a method for fabricating a thermally-enhanced wafer-level chip scale package, including steps of: preparing a semiconductor wafer predefined into a plurality of integrated circuit chips; *then* performing a bumping process; *then* performing a back-side lapping process to grind away a back-side portion of the semiconductor wafer; *then* attaching a thermally-conductive stiffener to the back side of the semiconductor wafer; *then* performing a singulation process to cut the thermally-conductive stiffener and cut apart each chip from the semiconductor wafer; and *then* performing a flip-chip die bonding process. As amended, claim 1 requires that the above steps must be performed in this order.

In particular, the bumping process is performed **prior** to the back-side lapping/grinding process for the wafer. Claim 1 also recites a step of performing a singulation process to cut the thermally-conductive stiffener and cut apart each chip from the semiconductor wafer *in a single step*. This step is shown in FIG. 5 of the application, as described, e.g., on page 5, line 24 to page 6, line 2.

Claims 1 and 3 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 6,392,290 to Kasem et al. ("Kasem"). Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Kasem in view of U.S. Patent 6,403,882 to Chen et al. ("Chen"). Claim 4 was rejected under 35 USC 103(a) as being unpatentable over Kasem in view of U.S. Patent 6,550,531 to Searls et al. These rejections are respectfully traversed.

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Kasem does not teach or suggest a fabrication method in which a bumping process is performed prior to a back-side lapping/grinding process. Kasem also does not teach or suggest the step of performing a singulation process to cut a thermally-conductive stiffener and cut apart each chip in a single step.

In Kasem, a method for fabricating a package includes steps performed in the following order. First, a chip 220 is prepared (see column 9, line 24 to column 10, line 13; and FIGS. 47A-53C). Then, a semiconductor substrate 227 of the chip 220 is thinned by grinding its back side (see column 10, lines 14-21; and FIGS. 54A-54C). Then, a heat sink 245 is bonded to the back side of the thinned substrate 227 using an adhesive layer 246 (see column 10, lines 23-26; and FIGS. 55A-55C). Then, solder bumps 248 are formed over a front side of the chip 220 (see column 10, lines 30-34; and FIGS. 56A-56C). Then, the substrate 227 is sawed at locations 250 "to separate it from the portions of the substrate in other chips on the wafer. **The heat sink 245 is left intact**" (column 10, lines 35-38 (emphasis added); FIGS. 57A-57C). Finally, the chip 220 is separated from other chips in the wafer by sawing through the heat sink 245 at locations 252 (see column 10, lines 40-42; and FIGS. 58A-58C).

In the method of Kasem, as described above, the step of forming solder bumps 248 occurs after a step of lapping/grinding the substrate 227. In contrast, the Applicants' claimed invention requires a bumping process to be performed prior to a back-side lapping process.

Also, in Kasem, the heat sink 245 "is left intact" during a step of sawing the substrate 227, and a further sawing step is required to separate the chip 220 from other chips. However, in the Applicants' claimed invention, the singulation process requires cutting a thermally-conductive stiffener and cutting apart each chip *in a single step*.

For at least the reasons discussed above, the Kasem reference does not anticipate or otherwise render obvious the Applicants' claimed invention.

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It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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